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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Bruno GHYSELEN et al.

Confirmation No.: 9199

Patent No.: 7,008,857 B2

Application No.: 10/764,289

Patent Date: March 7, 2006

Filing Date: January 23, 2004

For: RECYCLING A WAFER COMPRISING
A BUFFER LAYER, AFTER HAVING
SEPARATED A THIN LAYER
THEREFROM

Attorney Docket No.: 4717-8500

**REQUEST FOR CERTIFICATE OF CORRECTION
UNDER 37 C.F.R. §§ 1.322 AND 1.323**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**Certificate
MAR 27 2006
of Correction**

Sir:

Patentees hereby respectfully request the issuance of a Certificate of Correction in connection with the above-identified patent. The corrections are listed on the attached Form PTO-1050. The corrections requested are as follows:

Title Page:

Item (75) Inventors, after "Yves-Mathieu", change "Vaillant" to -- Le Vaillant --. The inventor's name will then correctly appear as "Yves-Mathieu Le Vaillant". Support for this change appears on the Declaration filed September 72, 2004

Item (56) References Cited, Other Publications, "Q.Y. Tong et al." reference, before "Wiley & Sons, Inc.", change "Johnson" to -- John --. This change is requested merely to correct an inadvertent clerical error.

Column 28:

Line 47 (claim 12, line 7), after "(c)", change "hiP" to -- InP --. Support for this change appears in original application claim 12

MAR 28 2006

The requested changes are to correct errors of a clerical or typographical nature and do not involve changes that would constitute new matter or require reexamination.

A fee of \$100 is believed to be due for this request. Please charge the required fees to Winston & Strawn LLP Deposit Account No. 50-1814. Please issue a Certificate of Correction in due course.

Respectfully submitted,

3-23-06

Date

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.: 7,008,857 B2
DATED: March 7, 2006
INVENTORS: Ghyselen et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page:

Item (75) Inventors, after "Yves-Mathieu", change "Vaillant" to -- Le Vaillant --.

Item (56) References Cited, Other Publications, "Q.Y. Tong et al." reference, before "Wiley & Sons, Inc.", change "Johnson" to -- John --.

Column 28:

Line 47, after "(c)", change "hiP" to -- InP --.



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(12) **United States Patent**
Ghyselen et al.

(10) **Patent No.:** **US 7,008,857 B2**
 (45) **Date of Patent:** ***Mar. 7, 2006**

(54) **RECYCLING A WAFER COMPRISING A
 BUFFER LAYER, AFTER HAVING
 SEPARATED A THIN LAYER THEREFROM**

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(*) **Notice:** Subject to any disclaimer, the term of this
 patent is extended or adjusted under 35
 U.S.C. 154(b) by 39 days.

This patent is subject to a terminal dis-
 claimer.

(21) **Appl. No.:** **10/764,289**

(22) **Filed:** **Jan. 23, 2004**

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 filed on Aug. 26, 2003.

(60) Provisional application No. 60/431,928, filed on Dec.
 9, 2002.

Foreign Application Priority Data

Aug. 26, 2002 (FR) 02 10587

(51) **Int. Cl.**
H01L 21/46 (2006.01)

(52) **U.S. Cl.** 438/455; 438/458; 438/406

(58) **Field of Classification Search** 438/455-459,
 438/406, 507

See application file for complete search history.

(56) References Cited

U.S. PATENT DOCUMENTS

5,854,123 A * 12/1998 Sato et al. 438/507
 5,882,987 A 3/1999 Srikrishnan 438/458
 5,966,620 A * 10/1999 Sakaguchi et al. 438/455
 6,143,628 A * 11/2000 Sato et al. 438/455

(Continued)

FOREIGN PATENT DOCUMENTS

EP 0 849 788 A2 6/1998

(Continued)

OTHER PUBLICATIONS

L. J. Huang et al, "SiGe-on-insulator prepared by wafer
 bonding and layer transfer for high-performance field-effect
 transistors", Applied Physics Letters, vol. 78, No. 9, pp.
 1267-1269 (2001).

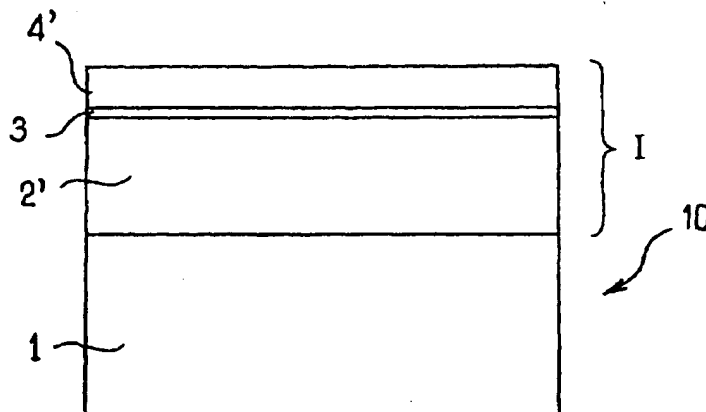
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(57) ABSTRACT

A method of recycling a donor wafer after detaching at least
 one useful layer is provided, the donor wafer comprising
 successively a substrate, a buffer structure and, before
 detachment, a useful layer. The method includes removal of
 substance relating to part of the donor wafer on the side
 where the detachment took place, such that, after removal of
 substance, there remains at least part of the buffer structure
 capable of being reused as at least part of a buffer structure
 during a subsequent detachment of a useful layer. The
 present document also relates to a method of producing a
 donor wafer which can be recycled according to the inven-
 tion, methods of detaching a thin layer from a donor wafer
 which can be recycled according to the invention, and donor
 wafers which can be recycled according to the invention.

36 Claims, 4 Drawing Sheets



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U.S. PATENT DOCUMENTS

6,146,979 A * 11/2000 Henley et al. 438/458
 6,159,824 A * 12/2000 Henley et al. 438/455
 6,284,628 B1 9/2001 Kuwahara et al. 438/459
 6,306,729 B1 10/2001 Sakaguchi et al. 438/458
 6,326,279 B1 * 12/2001 Kakizaki et al. 438/406
 6,375,738 B1 4/2002 Sato 117/89
 6,468,923 B1 10/2002 Yonehara et al. 438/761
 2001/0003269 A1 6/2001 Wu et al. 117/94
 2001/0029072 A1 10/2001 Kuwahara et al. 438/151
 2002/0068419 A1 6/2002 Sakaguchi et al. 438/458
 2002/0072130 A1 6/2002 Cheng et al. 438/10
 2003/0124815 A1 7/2003 Henley et al. 438/460
 2003/0159644 A1 8/2003 Yonehara et al. 117/8
 2004/0006311 A1 1/2004 Shchervinsky 604/164.01

FOREIGN PATENT DOCUMENTS

EP 0 926 709 A2 6/1999
 EP 0 955 671 A1 11/1999
 EP 1006 567 A2 6/2000
 EP 1 039 513 A2 9/2000
 WO WO 99/53539 10/1999
 WO WO 01/11930 A2 2/2001

OTHER PUBLICATIONS

Q. Y. Tong et al "Extracts of Semi-conductor on wafer bonding", Science and Technology, Interscience Technology, Wiley Interscience publication, Johnson Wiley & Sons, Inc.

* cited by examiner

John

After recycling, the donor wafer 10 includes:

a substrate 1 comprising AsGa at its interface with the buffer structure I;

a buffer structure I comprising InGaAs;

an InP protective layer 3 located on or in the InGaAs.

In a first scenario, the selective chemical etching of the InGaAs overlying the protective layer 3 with a selective etching solution, such as a solution comprising $\text{Ce}^{IV} \text{H}_2\text{SO}_4$, makes it possible to take off virtually all of this material overlying the protective layer 3, the protective layer 3 behaving here like an etching stop layer.

In a second scenario, after removing the InGaAs overlying the protective layer 3, the selective chemical etching of the protective layer 3 with a selective etching solution, such as a solution comprising HF, makes it possible to take off virtually all of the protective layer 3, the InGaAs underlying the protective layer 3 behaving here like an etching stop layer.

In a third scenario, it is possible for two selective etchings to succeed one another in order to remove part of the InGaAs and to remove the protective layer 3.

In the semiconductor layers presented in this document, other components may be added to them, such as carbon with a carbon concentration substantially less than or equal to 50% or more particularly with a concentration less than or equal to 5% in the layer in question.

Finally, the present invention is not limited to a buffer structure I, an intermediate layer 8 or an overlayer 5 made of materials presented in the examples above, but extends also to other alloys of Groups IV—IV, III-V, or II-VI.

It should be specified that these alloys may be binary, ternary, quaternary or of a higher degree.

The present invention is not limited either to a recyclable buffer layer 2 or buffer structure I having the prime function of matching the lattice parameter between two adjacent structures with different respective lattice parameters, but also relates to any buffer layer 2 or buffer structure I as defined in the most general manner in the present document and which can be recycled according to the invention.

The structures finally obtained after detachment are not limited either to SGOI, SOI, SiSGOI structures, or to structures for HEMT and HBT transistors.

As can be seen, the present invention, as described above and shown in the drawings, provides for a more economical method for recycling a wafer than with prior art techniques.

It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention include all such modifications and variations within the scope of the appended claims and their equivalents.

What is claimed is:

1. A method of recycling a donor wafer after detachment of a useful layer of a semiconductor material therefrom, wherein the donor wafer, after detachment of the useful layer, includes a substrate, a buffer structure on the substrate and a remaining portion of the useful layer, which method comprises removing at least part of the remaining portion of the useful layer in order to provide a donor wafer surface that is suitable for use in a subsequent detachment of a new useful layer.

2. The method of claim 1, wherein the remaining portion of the useful layer is removed chemically.

3. The method of claim 2, wherein the remaining portion of the useful layer is removed by selective chemical etching.

4. The method of claim 3, wherein the selective chemical etching includes at least one etching fluid having an etching power which is substantially greater for the useful layer than for the buffer structure, so that the buffer structure acts as an etching stop layer for the at least one etching fluid.

5. The method of claim 4, wherein the buffer structure comprises a material that differs from that of the useful layer in that:

the materials are different;

the materials contain atomic elements which are substantially identical except for at least one atomic element; the materials or each are substantially identical, but at least one atomic element in one material has an atomic concentration which is substantially different from that of the same atomic element in the other material; or the materials have different porosity densities.

6. The method of claim 2, wherein the chemical etching is preceded, followed or both preceded and followed by a mechanical eroding of the wafer surface.

7. The method of claim 6, wherein the mechanical eroding includes polishing, grinding or abrasion.

8. The method of claim 1, wherein, before detachment, the buffer structure includes a buffer layer and an additional layer that has (a) a thickness which is sufficient to contain defects therein or (b) a surface lattice parameter which is substantially different from that of the substrate.

9. The method of claim 8, wherein the mechanically removing includes removing all of the remaining portion of the useful layer and part of the additional layer or all of the additional layer and part of the buffer layer.

10. The method of claim 1, which further comprises providing at least one new layer on the donor wafer after removing at least part of the remaining portion of the useful layer so as to form a new useful layer or new buffer structure above the existing buffer structure.

11. The method of claim 10, which further comprises, before detachment, providing the donor wafer with an overlayer which includes the useful layer to be detached, and wherein the mechanically removing removes any portion of the overlayer that remains after detachment.

12. The method of claim 11, wherein the overlayer includes

(a) a material selected from the group consisting of SiGe and strained Si;

(b) a material selected from the group consisting of AsGa and Ge; or

(c) ~~hiP~~ or another alloy of Group III V elements.

InP

13. ~~The method of claim 10, which further comprises~~ providing at least two new layers on the donor wafer after removing at least part of the remaining portion of the useful layer so as to form an interlayer between the buffer structure and the new useful layer, with the interlayer optionally being provided by layer growth.

14. The method of claim 13, wherein the interlayer includes

(a) a material selected from the group consisting of SiGe and strained Si;

(b) a material selected from the group consisting of AsGa and/or Ge;

(c) an alloy of Group III V elements; or

(d) a material selected from the group consisting of InP and a Group III-V material having a lattice parameter substantially identical to that of InP.

15. The method of claim 13, wherein the buffer structure has a composition that includes an atomic alloy of binary, ternary, quaternary or of higher degree, selected from the